A Comparative Study of AC Positive Bias Temperature Instability of Germanium nMOSFETs with GeO_2/Ge and Si-cap/Ge Gate Stack

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ABSTRACT AC positive bias temperature instability (PBTI) of germanium nMOSFETs with GeO_2/Ge and Si-cap/Ge gate stack was investigated in this brief. AC-DC-AC alternating PBTI stress tests were conducted on both types of devices, the experiment data shows the inserted DC stress phase has little impact on the following AC stress kinetics on GeO_2/Ge nMOSFETs but introduce a significant "additional DC generation" on Si-cap/Ge devices. The "additional DC generation" is ascribed to the existence of energy alternating defects (EAD) according to previous studies. Energy distribution under DC and AC stress further demonstrate that EAD is significant on Si-cap/Ge but negligible on GeO_2/Ge devices. Effective lifetime prediction is carried out and compared under DC stress after discharge (with a purposely introduced measurement delay) and AC stress on both GeO_2/Ge and Si-cap nMOSFETs. The results show GeO_2/Ge nMOSFETs' effective lifetime exhibits no difference under two stress modes, while Si-cap/Ge nMOSFETs' effective lifetime is underestimated using DC stress after discharge approximation without considering the EAD-induced "additional DC generation". An extra 0.14V 10-year Vdd design margin can be obtained for Si-cap/Ge nMOSFETs to gain higher performance by taking "additional DC generation" into account. The conclusion is beneficial for process optimization and PBTI reliability improvement of Ge nMOSFETs.

INDEX TERMS AC PBTI, Germanium nMOSFETs, GeO_2/Ge, Si-cap/Ge, Energy Alternating Defects

I. INTRODUCTION

Owning to the higher bulk mobility of both hole and electron, germanium (Ge) possesses great potential to replace silicon (Si) in the channel of CMOS to enhance the carrier transport and consequently to achieve higher drive currents and switching speeds [1]. Ge MOSFETs used to suffer from the lack of a good native oxide which results in massive interface states, but significant progress has been made recently [2-9]. After good initial performance was achieved, attention has been paid to device reliability to pave the way for the debut of Ge CMOS. Bias temperature instability (BTI) of Ge MOSFETs, as the simplest and most common degradation mechanism, attracts massive attention [10-16].

The improvement of Ge MOSFETs was usually achieved through two routes: GeO_2 directly on Ge [2, 4, 7, 9] or using a Si capping layer [3, 8]. Previous studies reveal that GeO_2/Ge devices offer higher mobility for both p and n MOSFETs but suffer from poor reliability [16-18], while Si-capped devices exhibit a better NBTI reliability compared to Si counterpart [16]. The bulk of previous studies on Ge BTI adopted DC stress [10-15], and industry usually predicts AC BTI lifetime from DC stress after introducing a measurement delay either purposely [19] or unintentionally by using a measurement time of 10-100ms [20], as shown in Fig. 1a. The underlying justification is the hypothesis that degradation kinetics under effective AC stress time (stress time * duty factor) is the same

as DC stress kinetics after a delay-induced discharge. We have recently reported that this hypothesis is valid on SiON pMOSFETs but not applicable on GeO_2/Ge and Si-cap/Ge pMOSFETs subject to NBTI stress. The reason is that GeO_2/Ge and Si-cap/Ge pMOSFETs contain a lot of Energy Alternating Defects (EAD) [16] which result in a significant "additional DC generation" phenomenon and eventually lead to a significant AC effective lifetime underestimation, as shown in Fig. 1b (data from [16]). EAD were also observed on Si-cap/Ge nMOSFETs [12]. However, whether EAD also exists on GeO_2/Ge nMOSFETs, and how they impact the AC PBTI lifetime of Ge nMOSFETs, have not been studied yet.

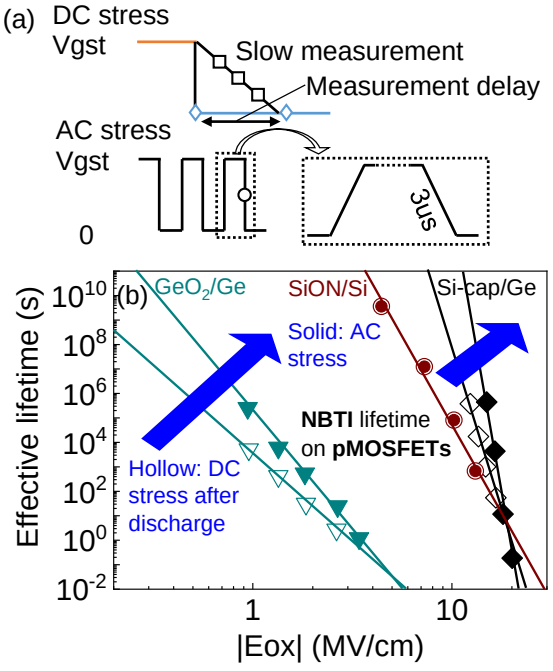

FIGURE 1. (a) Waveforms of DC stress after discharge (with measurement delay or slow measurement) and AC stress used for BTI lifetime prediction. (b) A replot of figure from [16], which shows the comparison of NBTI lifetime prediction on SiON, GeO_2 and Si-cap/Ge pMOSFETs. The blue arrows show the underestimation of AC effective lifetime due to "additional DC generation" compared to DC stress after discharge approximation.

In this work, a comparative study of AC PBTI of germanium nMOSFETs with GeO_2/Ge and Si-cap/Ge gate stack was carried out. AC-DC-AC alternating PBTI stress tests and energy distribution results clearly reveal that: GeO_2/Ge nMOSFETs have negligible EAD and EAD-induced "additional DC generation", while Si-cap nMOSFETs have significant EAD and exhibit clear "additional DC generation" phenomenon under DC stress after discharge stress compared to AC stress, resulting in an underestimation of AC effective lifetime if using conventional industry-adopted DC stress after discharge approximation.

II. DEVICES AND EXPERIMENTS

The schematic cross section of the two Ge nMOSFETs' gate stacks is shown in Fig. 2a. The fabrication process of the two types of nMOSFETs are as follows:

1) As for the GeO_2/Ge nMOSFET, a 700 nm Ge layer was prepared on a Si wafer, followed by oxidation at 150 ℃ in atomic oxygen to form 1.2 nm of GeO_2. A 4 nm Al_2O_3 layer was then deposited and the SiO_2 equivalent oxide thickness (EOT) is 2.35 nm. After the gate metallization with a 10 nm PVD TiN layer, the nMOSFETs were annealed in forming gas at 350 ºC for 20 min [18].

2) In terms of the Si-cap/Ge nMOSFET, Si-passivated Ge nMOSFETs were fabricated using a replacement metal gate high-k last process with the gate stack. After dummy gate removal and pre-cleaning, the thin Si layer was epitaxially grown on the Ge channel, followed by laser annealing at 750 ºC. The EOT of Si-cap/Ge nMOSFET is 1.40 nm [12].

Using Keysight B1530, arbitrary pulse waveform can be generated to achieve ultrafast pulse measurement. In this work, we employ a three microseconds pulse IV measured from the edge starting at the operating voltage (Vgop) and stopping at zero to monitor the degradation of threshold voltage (Vth), as shown in Fig. 2b. Due to the huge PBTI degradation on GeO_2/Ge nMOSFETs, constant overdrive stress voltage (Vgst_ov) was adopted to achieve a constant oxide electric field [21, 22] throughout all stress experiments, as illustrated in Fig. 2c. Unless specified, all the tests are carried out under 125 ºC and the AC stress frequency was 10 kHz with a duty factor of 0.5.

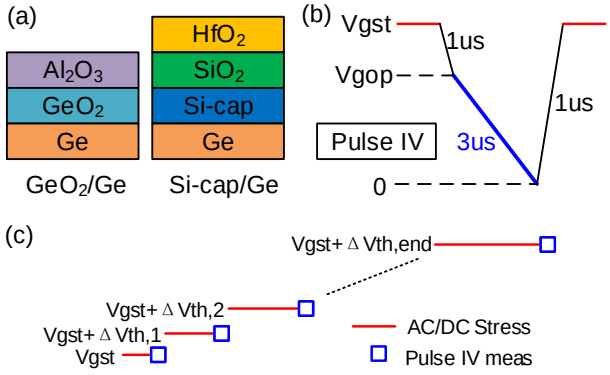

FIGURE 2. (a) Schematic cross section of the gate stacks of two types of Ge nMOSFET tested in this work. (b) Pulse IV from a 3us pulse edge was adopted to monitor the Vth. (c) Constant overdrive stress voltage (Vgst_ov) was adopted to achieve a constant oxide electric field throughout the stress tests.

III. RESULTS AND DISCUSSION

A. AC-DC-AC ALTERNATING STRESS KINETICS

A straight-forward way to evaluate the difference between DC and AC stress is monitoring the AC-DC-AC alternating stress kinetics on a single device, as shown in Fig. 3. Note for simplicity, constant Vgst_ov stress was adopted here but not

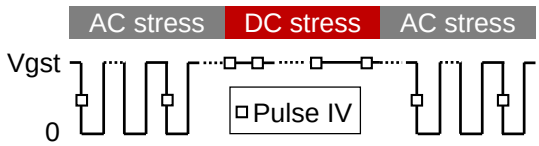

FIGURE 3. Illustration of AC-DC-AC alternating stress waveform. Constant Vgst_ov correction is not drawn for simplicity.

drawn in Fig. 3. Pulse IV measurements were taken at the end of ON stage during AC stress to capture the worst degradation. The whole experiment was accomplished within a single arbitrary waveform generated by B1530, without any test delay in the switch between AC and DC stress.

A typical test result of waveform in Fig. 3 on GeO_2/Ge nMOSFET was shown in Fig. 4a. Note due to the poor reliability of GeO_2/Ge nMOSFETs, the constant Vgst_ov correction could enhance the applied Vgst significantly as stress time evolves, hence Vgst_ov on GeO_2/Ge nMOSFETs cannot be set too high. Vgst_ov=1.1V AC stress was firstly applied and the degradation can be well fitted by a power law against effective stress time. After the 1st AC stress, a DC stress phase with the same Vgst_ov=1.1V was introduced, instantly enhanced ΔVth due to the trapping of recoverable defects which have a relatively long capture time thus cannot be charged during the 1st AC stress phase. After 1ks DC stress, the stress mode switched back to AC stress, resulting in an abrupt drop of ΔVth due to the detrapping of extra charged recoverable defects during DC stress. Most of the extra charged recoverable defects are discharged within 100s, as shown by the ceasing of slight ΔVth decrease in the 2nd AC stress kinetics. After that, AC stress induced degradation starts to take control and ΔVth slightly increases.

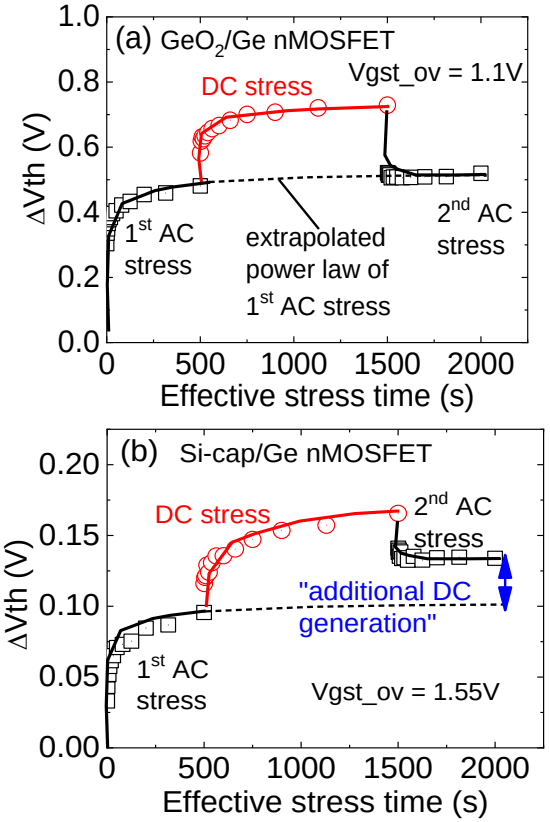

FIGURE 4. (a) On GeO_2/Ge device, the 2nd AC stress can fully recover DC-enhanced charging. (b) On Si-cap/Ge device, the 2nd AC stress cannot fully recover the additional defects generated from DC stress.

By extrapolating the power law of 1st AC stress, we observed that ΔVth in the latter half of 2nd AC stress can be well fitted by exactly the same power law of the 1st AC stress, implying the inserted DC stress has little impact on the subsequent AC stress on GeO_2/Ge nMOSFETs. A log-log plot is given in Fig. 5a to show this more clearly. Another AC-DC-AC stress kinetics subject to a lower Vgst_ov=0.5V was given to further confirm the observation.

The same test procedure was then performed on Si-cap/Ge nMOSFET, and the results were shown in Fig. 4b. Note due to Si-cap/Ge nMOSFETs possess much better reliability compared to GeO_2/Ge nMOSFETs, Vgst_ov adopted on Si-cap/Ge nMOSFETs is much higher than GeO_2/Ge nMOSFETs in order to induce enough ΔVth for clearer observation. In contrast to GeO_2/Ge nMOSFETs, the degradation in the latter half of 2nd AC stress is much higher than the extrapolated value from the 1st AC stress phase, as shown in Fig. 4b, indicating the DC stress phase had introduced an "additional DC generation" in the following AC stress phase. Another AC-DC-AC test results under Vgst_ov=1.1V are also given in Fig. 5b, further confirming the existence of "additional DC generation".

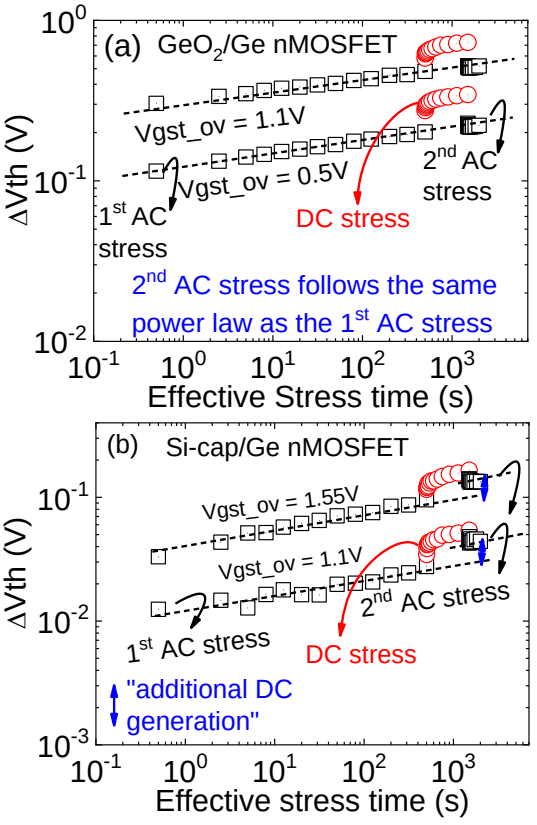

FIGURE 5. (a) On GeO_2/Ge device, the 2nd AC stress phase induced ΔVth in AC-DC-AC stress pattern follows the same generation kinetics as the 1st AC stress phase, suggesting no "additional DC generation" by the inserted DC stress phase. (b) On Si-cap/Ge device, the 2nd AC stress phase induced ΔVth in AC-DC-AC stress pattern is much higher than the extrapolated value from 1st AC stress phase, exhibiting an "additional DC generation" by the inserted DC stress phase.

The "additional DC generation" phenomenon and the difference between GeO_2/Ge and Si-cap/Ge nMOSFETs can be explained using the "As-grown Generation (A-G)" model [16, 23]. It has been reported that defects on Ge MOSFETs

can be categorized into three types: Generated Defects (GD), As-grown Traps (AT), and Energy Alternating Defects (EAD) [11, 12, 16, 24]. GD cannot discharge under 0V and follow the same generation kinetics against effective stress time under DC/AC stress [25], thus can be excluded from the origin of "additional DC generation". AT's trapping/detrapping is an elastic tunneling process, resulting in a memoryless charging/discharging kinetics hence should also be irrelevant to the "additional DC generation". In terms of EAD, according to the first-principles calculations, the basic mechanism of EAD is that, following charging, the defect will go through a lattice relaxation that leads to a lowering of the energy of the charged state so that it becomes more stable [26, 27]. The charging process of EAD can be elucidated using a double-well model [28], as shown in Fig. 6. EAD trapping is a two-step process, electrons must firstly overcome the 1st barrier, and then proceed to overcome the 2nd barrier by a field-enhanced relaxation process and reach the deep well [28]. The EAD trapped in the 2nd well is thus proportional to the charge density in the 1st well. The shallow level of the 1st well makes the charge density in the 1st well dynamic: it is much less under AC stress because of the short charging time and discharge at Vg=0V, eventually leads to less EAD in the 2nd well. In addition, AC ON time can be too short to complete the relaxation responsible for the EAD generation. This explains the missing "additional DC generation" on Si-cap/Ge nMOSFETs under AC stress. For GeO_2/Ge nMOSFETs, EAD is negligible compared to AT, thus manifest no difference between DC and AC stress. This also agree with the report in [12] that EAD in Si-cap/Ge nMOSFETs locate at SiO_2 layer close to the channel, which is missing in GeO_2/Ge structure nMOSFETs.

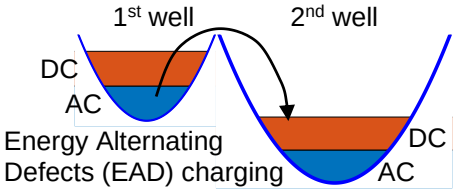

FIGURE 6. EAD charging process: EAD trapping in the 2nd well requires electrons in the 1st well to overcome the 2nd barrier, through a field-enhance relaxation process.

B. ENERGY DISTRIBUTION UNDER DC AND AC STRESS

The existence of EAD and EAD-induced "additional DC generation" on Si-cap/Ge nMOSFETs but not on GeO_2/Ge nMOSFETs could also be observed through the comparison of energy distribution of ΔVth under DC and AC stress. Based on the test-proven "Discharging-based Multiple Pulses (DMP)" technique [29, 30], we can extract the energy distribution of ΔVth on GeO_2/Ge and Si-cap/Ge nMOSFETs subject to DC stress. By replacing each DC charging and discharging phases with AC counterparts, the energy distribution of ΔVth subject to AC stress can then be obtained, as shown in Fig. 7. Note the charging/discharging time for AC is twice as the values in DC to keep the same effective charging/discharging time for a fair comparison.

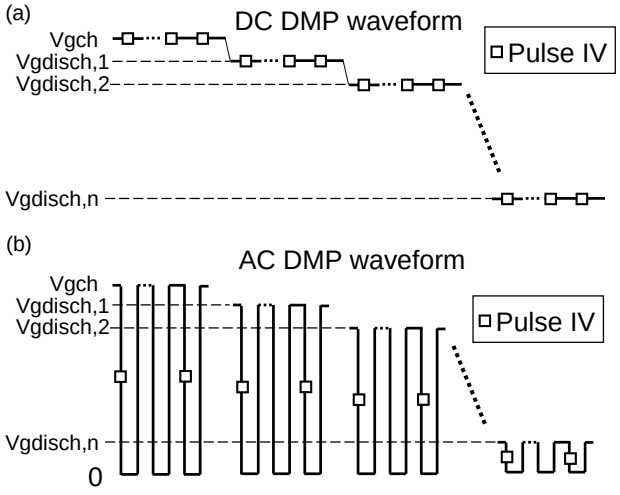

FIGURE 7. Illustration of the test waveform of DC and AC "Discharging-based Multiple Pulses (DMP)" technique to extract Δ Vth energy distribution.

A typical result of DC and AC energy distribution is shown in Fig. 8. Again we see on GeO_2/Ge nMOSFETs, DC and AC stress generate the same amount of GD with equivalent effective stress time, exhibits "no additional DC generation", while on Si-cap/Ge nMOSFETs, a significant "additional DC generation" is clearly observed.

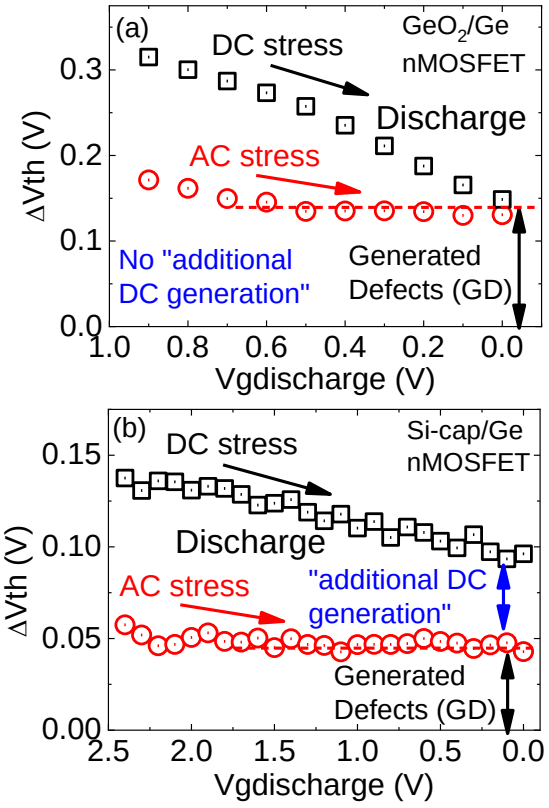

FIGURE 8. Comparisons of ΔVth energy distribution subject to DC and AC stress on (a) GeO_2/Ge nMOSFETs and (b) Si-cap/Ge nMOSFETs.

C. LIFETIME ANALYSIS

Due to the existence of EAD and EAD-induced "additional DC generation", Si-cap/Ge nMOSFETs' lifetime cannot be estimated from industry adopted DC stress after discharge approximation method. A comparison of lifetime prediction under AC stress and DC stress after discharge (by purposely insert a 1s measurement delay at 0V) was carried out on GeO_2/Ge and Si-cap/Ge nMOSFETs, as shown in Fig. 9-11. Note constant Vgst_ov stress was adopted for both stress modes, each Vgst_ov curve was obtained by averaging the stress kinetics on 3 devices to rule out the device variation.

Fig. 9 shows the degradation kinetics under DC stress after discharge and AC stress against effective stress time on GeO_2/Ge nMOSFETs. Clearly the two different stress modes exhibit exactly the same stress kinetics which can be well fitted by the traditional power law for BTI:

$$\Delta Vth = A \cdot Vgst\_ov^m \cdot t^n \quad (1)$$

Note the extra small Vgst_ov in Fig. 9 is in order to make the first ΔVth value (effective stress time = 1 s in Fig. 9) smaller than 100 mV, which is the typical failure criteria industry adopts for PBTI, to achieve an effective lifetime within the measurement window.

In contrast to GeO_2/Ge nMOSFETs, Si-cap/Ge nMOSFETs have the "additional DC generation" phenomenon thus DC stress after discharge stress kinetics (Fig. 10a) is higher compared to the AC stress counterpart (Fig. 10b) with the same Vgst_ov.

A comparison of effective lifetime prediction under DC stress after discharge and AC stress for GeO_2/Ge and Si-cap/Ge nMOSFETs at the failure criteria of ΔVth=100mV was shown in Fig. 10. Note the x-axis is discontinuous in the middle to show both effective lifetime clearly. To obtain an effective lifetime of 10 years, the maximum Eox projected by DC stress after discharge and AC stress is 6.26 MV/cm and 6.86 MV/cm, respectively. The corresponding 10-year overdrive Vdd is 1.47V and 1.61V. By considering the EAD-induced "additional DC generation", an extra 0.14V 10-year Vdd design margin is obtained for Si-cap/Ge nMOSFETs to gain higher performance.

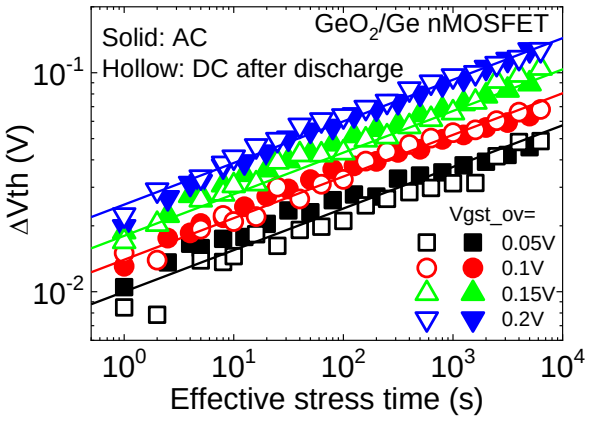

FIGURE 9. ΔVth under DC stress after discharge exhibits the same kinetics as AC stress on GeO_2/Ge nMOSFETs.

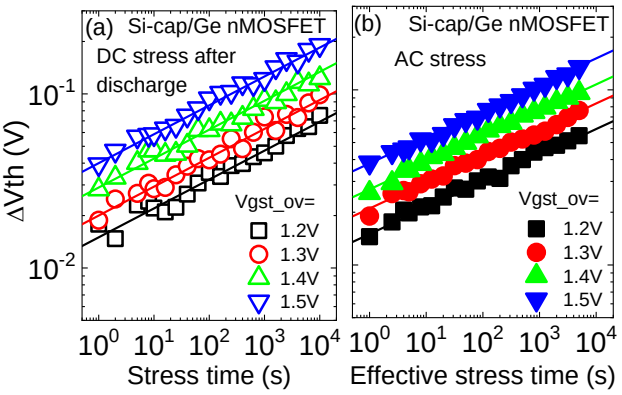

FIGURE 10. ΔVth under (a) DC stress after discharge is higher compared to (b) AC stress on Si-cap/Ge nMOSFETs.

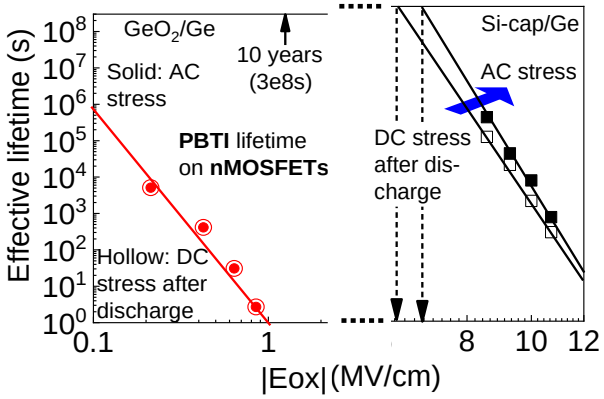

FIGURE 11. Comparisons of GeO_2/Ge and Si-cap/Ge nMOSFETs' predicted lifetime subject to DC stress after discharge and AC stress at the failure criteria of ΔVth=100mV. The x-axis is discontinuous in the middle for better view.

VI. CONCLUSION

A comparative investigation of AC PBTI of GeO_2/Ge and Si-cap/Ge nMOSFETs was conducted in this work. Our experiment results showed the major difference between GeO_2/Ge and Si-cap/Ge nMOSFETs' PBTI is Si-cap/Ge devices contain significant amount of EAD while GeO_2/Ge devices do not. The difference is speculated to be ascribed to the missing SiO_2 layer in GeO_2/Ge nMOSFETs according to previous studies. EAD's two-step charging process of EAD leads to an "additional DC generation" on Si-cap/Ge nMOSFETs, resulting in an underestimation of effective lifetime if conventional DC stress after discharge approximation method is adopted. The conclusion can be of great use for process optimization and PBTI reliability improvement of Ge nMOSFETs.

REFERENCES

[1] D. Kuzum, T. Krishnamohan, A. Nainani, Y. Sun, P. A. Pianetta, H.-S. P. Wong, and K. C. Saraswat, "High-mobility Ge N-MOSFETs and mobility degradation mechanisms," *IEEE Trans. Electron Devices*, vol. 58, no. 1, pp. 59-66, 2010.

[2] R. Zhang, T. Iwasaki, N. Taoka, M. Takenaka, and S. Takagi, "High-Mobility Ge pMOSFET With 1-nm EOT Al2O3/GeOx/Ge Gate Stack Fabricated by Plasma Post Oxidation," *IEEE Trans. Electron Devices*, vol. 59, no. 2, pp. 335-341, 2011.

[3] S. Sioncke, W. Vanherle, W. Art, J. Ceuppens, T. Ivanov, D. Lin, L. Nyns, A. Delabie, T. Conard, and H. Struyf, "Si cap passivation for Ge nMOS applications," *Microelectron. Eng.*, vol. 109, pp. 46-49, 2013.
[4] C. Lu, C. Lee, T. Nishimura, and A. Toriumi, "Design and demonstration of reliability-aware Ge gate stacks with 0.5 nm EOT," in *VLSI Symp. Tech. Dig.*, 2015, pp. T18-T19.
[5] J. Franco, B. Kaczer, A. Vais, A. Alian, H. Arimura, V. Putcha, S. Sioncke, N. Waldron, D. Zhou, and L. Nyns, "Bias Temperature Instability (BTI) in high-mobility channel devices with high-k dielectric stacks: SiGe, Ge, and InGaAs," *MRS Advances*, vol. 1, no. 49, pp. 3329-3340, 2016.
[6] A. Chasin, E. Bury, J. Franco, B. Kaczer, M. Vandemaele, H. Arimura, E. Capogreco, L. Witters, R. Ritzenthaler, H. Mertens, N. Horiguchi, and D. Linten, "Understanding the intrinsic reliability behavior of n-/p-Si and p-Ge nanowire FETs utilizing degradation maps," in *IEDM Tech. Dig.*, 2018, pp. 34.1.1-34.1.4.
[7] M. Ke, P. Cheng, K. Kato, M. Takenaka, and S. Takagi, "Characterization and understanding of slow traps in GeOx-based n-Ge MOS interfaces," in *IEDM Tech. Dig.*, 2018, pp. 34.3. 1-34.3. 4.
[8] H. Wan, Y. Hong, Y. Cheng, and M. Hong, "BTI Characterization of MBE Si-capped Ge gate stack and defect reduction via forming gas annealing," in *Proc. IRPS*, 2019, pp. 1-4: IEEE.
[9] M. Ke, M. Takenaka, and S. Takagi, "Reduction of Slow Trap Density in Al2O3/GeOxNy/n-Ge MOS Interfaces by PPN-PPO Process," *IEEE Trans. Electron Devices*, vol. 66, no. 12, pp. 5060-5064, 2019.
[10] B. Kaczer, J. Franco, J. Mitard, P. J. Roussel, A. Veloso, and G. Groeseneken, "Improvement in NBTI reliability of Si-passivated Ge/high-k/metal-gate pFETs," *Microelectron. Eng.*, vol. 86, no. 7-9, pp. 1582-1584, 2009.
[11] J. Ma, W. Zhang, J. F. Zhang, B. Benbakhti, Z. Ji, J. Mitard, J. Franco, B. Kaczer, and G. Groeseneken, "NBTI of Ge pMOSFETs: Understanding defects and enabling lifetime prediction," in *IEDM Tech. Dig.*, 2014, pp. 34.2.1-34.2.4.
[12] P. Ren, R. Gao, Z. Ji, H. Arimura, J. F. Zhang, R. Wang, M. Duan, W. Zhang, J. Franco, S. Sioncke, D. Cott, J. Mitard, L. Witters, H. Mertens, B. Kaczer, A. Mocuta, N. Collaert, D. Linten, R. Huang, A. V. Thean, and G. Groeseneken, "Understanding charge traps for optimizing Si-passivated Ge nMOSFETs," in *VLSI Symp. Tech. Dig.*, 2016, pp. 1-2.
[13] D. Kuzum, T. Krishnamohan, A. J. Pethe, A. K. Okyay, Y. Oshima, Y. Sun, J. P. McVittie, P. A. Pianetta, P. C. McIntyre, and K. C. Saraswat, "Ge-interface engineering with ozone oxidation for low interface-state density," *IEEE Electron Device Lett.*, vol. 29, no. 4, pp. 328-330, 2008.
[14] J. Franco, B. Kaczer, P. J. Roussel, J. Mitard, S. Sioncke, L. Witters, H. Mertens, T. Grasser, and G. Groeseneken, "Understanding the suppressed charge trapping in relaxed- and strained-Ge/SiO2/HfO2 pMOSFETs and implications for the screening of alternative high-mobility substrate/dielectric CMOS gate stacks," in *IEDM Tech. Dig.*, 2013, pp. 15.2.1-15.2.4.
[15] G. Groeseneken, J. Franco, M. Cho, B. Kaczer, M. Toledano-Luque, P. Roussel, T. Kauerauf, A. Alian, J. Mitard, and H. Arimura, "BTI reliability of advanced gate stacks for Beyond-Silicon devices: Challenges and opportunities," in *IEDM Tech. Dig.*, 2014, pp. 34.4. 1-34.4. 4: IEEE.
[16] J. Ma, W. Zhang, J. F. Zhang, Z. Ji, B. Benbakhti, J. Franco, J. Mitard, L. Witters, N. Collaert, and G. Groeseneken, "AC NBTI of Ge pMOSFETs: Impact of energy alternating defects on lifetime prediction," in *VLSI Symp. Tech. Dig.*, 2015, pp. T34-T35.
[17] K. Morii, T. Iwasaki, R. Nakane, M. Takenaka, and S. Takagi, "High performance GeO2/Ge nMOSFETs with source/drain junctions formed by gas phase doping," in *IEDM Tech. Dig.*, 2009, pp. 1-4: IEEE.
[18] J. Ma, J. F. Zhang, Z. Ji, B. Benbakhti, W. Zhang, J. Mitard, B. Kaczer, G. Groeseneken, S. Hall, J. Robertson, and P. Chalker, "Energy Distribution of Positive Charges in Al2O3/GeO2/Ge pMOSFETs," *IEEE Electron Device Lett.*, vol. 35, no. 2, pp. 160-162, 2014.
[19] Intel, *Quality System Handbook*. 2009, pp. 19-22.
[20] V. Huard and M. Denais, "Hole trapping effect on methodology for DC and AC negative bias temperature instability measurements in PMOS transistors," in *Proc. IRPS*, 2004, pp. 40-45: IEEE.
[21] R. Gao, A. B. Manut, Z. Ji, J. Ma, M. Duan, J. F. Zhang, J. Franco, S. W. M. Hatta, W. D. Zhang, B. Kaczer, D. Vigar, D. Linten, and G. Groeseneken, "Reliable Time Exponents for Long Term Prediction of Negative Bias Temperature Instability by Extrapolation," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1467-1473, 2017.
[22] R. Gao, Z. Ji, J. F. Zhang, J. Marsland, and W. D. Zhang, "As-grown-Generation Model for Positive Bias Temperature Instability," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3662-3668, 2018.
[23] R. Gao, Z. Ji, S. M. Hatta, J. F. Zhang, J. Franco, B. Kaczer, W. Zhang, M. Duan, S. D. Gendt, D. Linten, G. Groeseneken, J. Bi, and M. Liu, "Predictive As-grown-Generation (A-G) model for BTI-induced device/circuit level variations in nanoscale technology nodes," in *IEDM Tech. Dig.*, 2016, pp. 31.4.1-31.4.4.
[24] J. Ma, W. D. Zhang, J. F. Zhang, B. Benbakhti, Z. Ji, J. Mitard, and H. Arimura, "A Comparative Study of Defect Energy Distribution and Its Impact on Degradation Kinetics in GeO2/Ge and SiON/Si pMOSFETs," *IEEE Trans. Electron Devices*, vol. 63, no. 10, pp. 3830-3836, 2016.
[25] Z. Ji, J. F. Zhang, L. Lin, M. Duan, W. Zhang, X. Zhang, R. Gao, B. Kaczer, J. Franco, T. Schram, N. Horiguchi, S. D. Gendt, and G. Groeseneken, "A test-proven As-grown-Generation (A-G) model for predicting NBTI under use-bias," in *VLSI Symp. Tech. Dig.*, 2015, pp. T36-T37.
[26] D. Liu, Y. Guo, L. Lin, and J. Robertson, "First-principles calculations of the electronic structure and defects of Al2O3," *J. Appl. Phys.*, vol. 114, no. 8, p. 083704, 2013.
[27] J. Weber, A. Janotti, and C. Van de Walle, "Native defects in Al2O3 and their impact on III-V/Al2O3 metal-oxide-semiconductor-based devices," *J. Appl. Phys.*, vol. 109, no. 3, p. 033715, 2011.
[28] T. Grasser, B. Kaczer, W. Goes, T. Aichinger, P. Hehenberger, and M. Nelhiebel, "A two-stage model for negative bias temperature instability," in *Proc. IRPS*, 2009, pp. 33-44.
[29] S. W. M. Hatta, Z. Ji, J. F. Zhang, M. Duan, W. D. Zhang, N. Soin, B. Kaczer, S. De Gendt, and G. Groeseneken, "Energy Distribution of Positive Charges in Gate Dielectric: Probing Technique and Impacts of Different Defects," *IEEE Trans. Electron Devices*, vol. 60, no. 5, pp. 1745-1753, 2013.
[30] X. F. Zheng, W. D. Zhang, B. Govoreanu, J. F. Zhang, and J. V. Houdt, "A discharge-based multi-pulse technique (DMP) for probing electron trap energy distribution in high-k materials for Flash memory application," in *IEDM Tech. Dig.*, 2009, pp. 1-4.